

UCC27714 High-Speed, 600-V High-Side Low-Side Gate Driver with 4-A Peak Output

1 Features

- High-Side, Low-Side Configuration, with Independent Inputs
- Fully Operational up to 600 V (HS Pin)
- Floating Channel Designed for Bootstrap Operation
- Peak Output Current Capability of 4-A Sink 4-A Source at $V_{DD} = 15\text{ V}$
- Best-In-Class Propagation Delay (90 ns Typical, 125 ns Maximum)
- Best-In-Class Delay Matching (20 ns Maximum)
- TTL and CMOS Compatible Input Logic
- V_{DD} Bias Supply Range of 10 V to 20 V
- Bias UVLO Protection for Both Channels
- Rail-to-Rail Drive
- Robust Operation Under Negative Voltage Transients
- High dv/dt Immunity (HS Pin)
- Separated Grounds for Logic (V_{SS}) and Driver (COM) with Capability to Sustain Voltage Difference

2 Applications

- Half-Bridge and Full-Bridge Converters in Offline AC and DC Power Supplies
- High-Density Switching Power Supplies for Server, Telecom, IT and Industrial Infrastructure
- Solar Inverters, Motor Drive and UPS

3 Description

UCC27714 is a 600-V high-side, low-side gate driver with 4-A source and 4-A sink current capability, targeted to drive power MOSFETs or IGBTs. The device comprises of one ground-referenced channel (LO) and one floating channel (HO) which is designed for operating with bootstrap supplies. The device features excellent robustness and noise immunity with capability to maintain operational logic at negative voltages of up to -8 V_{DC} on HS pin (at $V_{DD} = 12\text{ V}$).

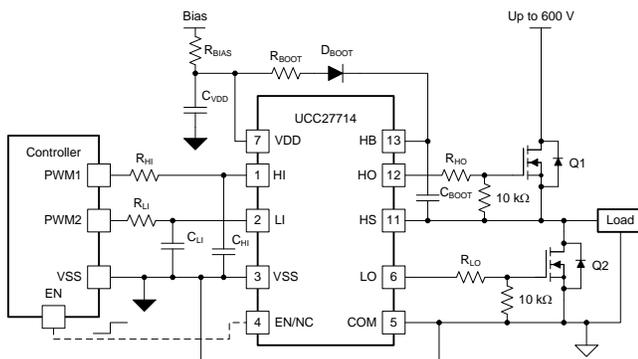
The device accepts a wide range bias supply input from 10 V to 20 V and offers UVLO protection for both the VCC and HB Bias supply pins. UCC27714 is available in SOIC-14 package and rated to operate from -40°C to 125°C .

Device Information⁽¹⁾

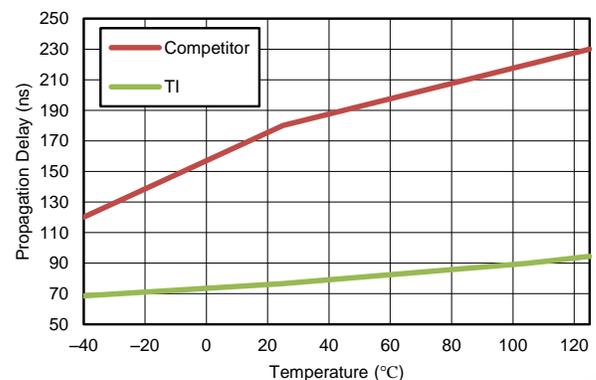
PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27714	SOIC (14)	

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Typical Propagation Delay Comparison



5 Device and Documentation Support

5.1 Trademarks

All trademarks are the property of their respective owners.

5.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

5.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27714D	PREVIEW	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC27714	
UCC27714DR	PREVIEW	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC27714	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

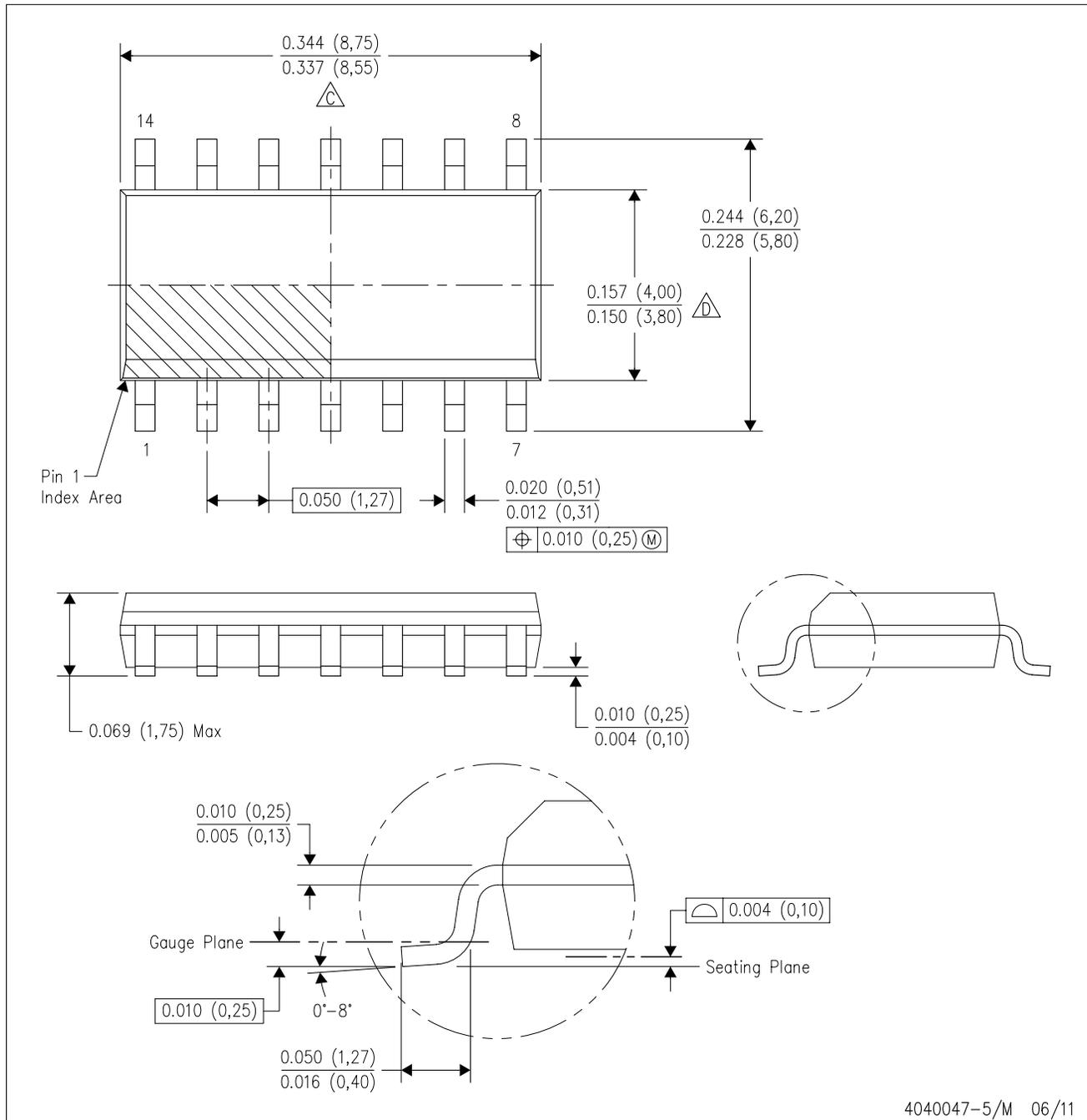
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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D (R-PDSO-G14)

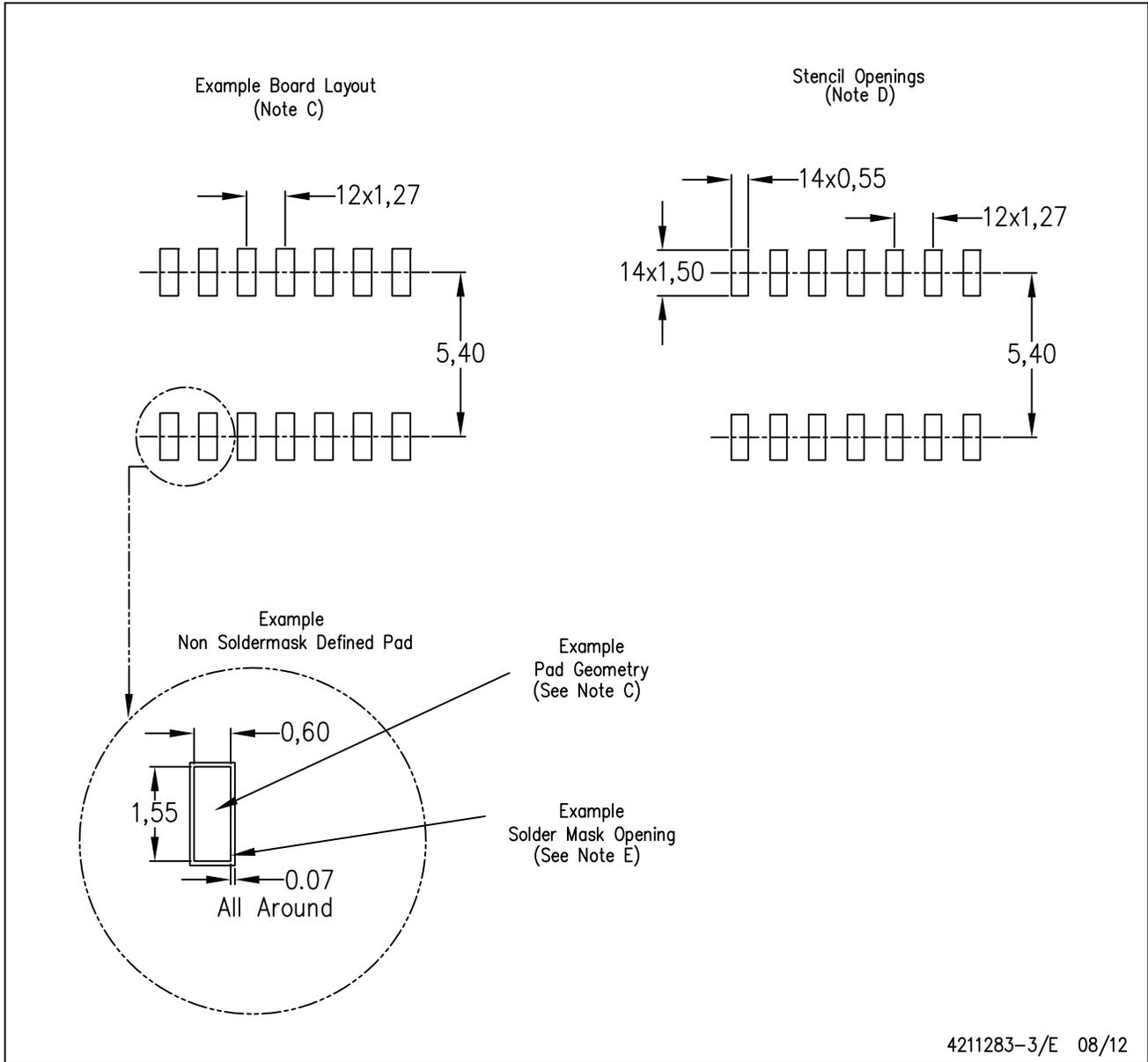
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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